

REMARKS

This paper responds to the Office Action mailed on December 13, 2004.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

§112 Rejection of the Claims

Claims 11-25, 35-39, and 41-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant respectfully submits that the amendments to independent claims 11, 15, 18, 22, 25, 35 and 41, contained herein, place the rejected claims in patentable condition. The Examiner states that the limitation “that a structure’s dimension is “reduced” from an earlier dimension during a “process,” without any clear way knowing what the reduction was by looking at the final structure” does not clearly distinguish from the prior art structure. Applicant submits that the amended phrasing of “*...with a top portion of each individual planar perimeter side surface disposed in the second region and within approximately 5 microns of an edge of the first region ...*”, as recited in claim 11, and similar phrasing in the other independent claims, does provide a clear way of distinguishing the final structure from other structures.

The amendments discussed above find support in the specification, for example, in figures 2 and 3, and on page 5, lines 18-20 and 27-29; page 5, lines 27-29; and page 7, lines 4-12. In view of the above noted amendments to the independent claims Applicant respectfully requests that this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 11-16, 18-25, 35-38, and 41-43 were rejected under 35 USC § 103(a) as being unpatentable over Boruta (EP 06478904A1) in view of Camasta (U.S. Patent No. 3,545,325), Baker et al. (U.S. Patent No. 3,689,803) and Weisshaus et al. (Dicing article). Applicant respectfully traverses this rejection.

The cited references have features discussed in the previous response, which is incorporated herein by reference. Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of “*...each planar perimeter side surface of the semiconductor die being a polished surface with a top portion of each individual planar perimeter side surface disposed in the second region and within approximately 5 microns of an edge of the first region ...*”, as recited in independent claim 11, as amended herein. The outstanding Office Action admits that the cited reference of Boruta does not describe or suggest polishing the side surfaces of the IC, and further Applicant submits that there is no suggestion in the cited reference of polishing the side surface to a point close to the active area of the IC. If the dicing apparatus of the cited Camasta reference is to be used as suggested by the Examiner as the “polishing” apparatus of the claimed invention, then one of ordinary skill in the art would be forced to the conclusion that the distance between the active area devices and the suggested “polished” edge would of necessity be 50 to 100 microns since that is approximately half of the typical scribe line width. Thus the result of the suggested combination of Boruta and Camasta might then be one IC die with four scribe line cuts that are near the active region, while the eight surrounding IC die will have scribe lines that are up to 100 microns wide. The other two cited references are not seen as curing the above noted deficiency in the combination of Boruta and Camasta.

Applicant respectfully submits that the suggested combination of references can not suggest to one of ordinary skill in the art the benefit of reducing the scribe line width since the references relate to dicing operations and alignment tolerances and disclose cutting the center of the scribe line, and do not suggest polishing the initial dice cut to remove defects and to reduce the final IC die size. Thus independent claim 11, as amended herein, is held to be patentable over the suggested combination of references.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of “*...with a top portion of each individual planar perimeter side surface disposed in the second region and within approximately 5 microns of an edge of the first region ...*”, as recited in independent claim 15, as amended herein. The reasons are similar to those given above with reference to the rejection of claim 11.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of “*...with a top portion of an upper one of the one or more perimeter side surfaces disposed in the second region and within approximately 5 microns of an edge of the first region ...*”, as recited in independent claim 18, as amended herein. The reasons are similar to those given above with reference to the rejection of claims 11 and 15.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of “*...with a top portion of an upper one of the one or more perimeter sides disposed in the second region and within approximately 5 microns of an edge of the first region ...*”, as recited in independent claim 22, and substantially similar language in independent claims 25, 35 and 41, as amended herein. The reasons are similar to those given above with reference to the rejection of claims 11, 15 and 18.

The independent claims have been shown above to be patentable over the suggested combination of references because of the feature of dicing the wafer and polishing the sidewalls to close to the active area of the IC. This operation results in a die that has fewer defects caused by the rapid slicing of the scribe saw operation, and reduces the overall die size. The dependent claims are believed to be in patentable condition at least as depending upon base claims shown above to be patentable over the suggested combination of references.

In view of the above discussed amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

SUPPLEMENTARY AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116

Serial Number: 09/785,006

Filing Date: February 16, 2001

Title: GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorneys, Tim Clise at (612) 349-9587 or David Suhl (508) 865-8211 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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Date

11 May '05

By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of May, 2005.

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